Customer No.: 31561
Application No.: 10/063,737
Docket No.: 8727-US-PA

REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 16-22. Specifically, the Office Action rejected claims 16-22 under 35 U.S.C. 103(a), as being unpatentable over Sharma et al. (US 5,990,547) in view of Brooks et al. (US 6,326,244). Further, the Office Action rejected claims 16-22 under 35 U.S.C. 102(b) as being anticipated by Honsinger et al. (US 5,500,804) in view of Brooks. Applicant respectfully requests reconsideration of those claims and newly added claims 27-33.

Discussion of Office Action Rejections

The Office Action rejected claims 16-22 under 35 U.S.C. 103(a), as being unpatentable over Sharma et al. (US 5,990,547) in view of Brooks et al. (US 6,326,244). Applicant respectfully traverses the rejections for at least the reasons set forth below.

Combination of Sharma in view of Brooks does not teach, disclose or suggest the feature of ""a non-signaling layer having a voltage reference signal trace, wherein the voltage reference signal trace is wider than the other signal traces". More specifically, as disclosed in column 3, lines 55-56 of Sharma, on which the Examiner relies to reject the present application, "... the layers 4 and 6 are voltage reference layers which in a specific embodiment include a ground layer and a power layer ...". Further, as shown in FIG. 3 and column 3, lines 62-64 of Sharma, "... The trace 28 in turn, is connected to a via 30 which makes contact with an isolated trace 32 at routing layer 4 ...". However, as described in column 3, lines 65-67, "... The trace 32 in turn makes contact with the via 34 which is a through hole via. The through hole via 34 makes contact to both of the plating buses 36 and 38", the isolated trace 32 is used to connect plating buses to the traces going to be plated, such as solder pad 16, 19, 51 or the bond posts 27 (column 3, lines 49-52), *the isolated trace 32 is not the voltage reference signal trace as claimed in claim 16 of the present invention*. Further, Brooks does not teach, disclose or suggest a non-

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signaling layer having a voltage reference signal trace. Accordingly, **combination of Sharma and Brooks does not disclose a voltage reference layer having a voltage reference signal trace.** Therefore, claim 16 is patentable over Sharma in view of Brooks.

Accordingly, claims 17-22 are patentable over Sharma in view of Brooks as a matter of law since claim 16, which is depended by claims 17-22, is patentable over Sharma in view of Brooks.

The Office Action further rejected claims 16-22 under 35 U.S.C. 102(b) as being anticipated by Honsinger in view of Brooks. Applicants respectfully traverse the rejections for at least the reasons set forth below.

To anticipate a claim, the reference must teach each and every element of the claim. M.P.E.P. § 2131. However, neither Honsinger nor Brooks disclose the feature of "a non-signaling layer having a voltage reference signal trace, wherein the voltage reference signal trace is wider than the other signal traces" as claimed in claim 16. According to column 4, lines 12-15, on which the Office Action relied to reject the present application, wiring media layers are typically arranged as wiring layer pairs with a voltage reference layer. However, in column 3, line 64 - column 4, line 33, on which the Examiner relies to reject the present application, *not any voltage reference traces exist in the voltage reference layer*. Further, Brooks did not teach, disclose or suggest the same feature. Accordingly, those skilled in the art are not taught to design voltage reference signal trace into the voltage reference layer according to Honsinger or Brooks.

For at least the reasons stated above, it is obvious that Honsinger in view of Brooks did not teach each and every element of claim 16. Therefore, claim 16 is patentable over Honsinger in view of Brooks.

Claims 17-22 are therefore patentable over Honsinger as a matter of law since their depending claim 16 is patentable over Honsinger.

The newly added claims 27-33 are patentable over the citations. More specifically, the citations do not teach, disclose or suggest the feature of "... a non-signaling layer having a voltage reference signal trace with a constant voltage input;" as claimed in claim 27.

Here, the "constant voltage" is also known as a reference voltage (i.e. see paragraph [0004]), and does not raise new mater.

As stated in Sharma, trace 32 is used to connect the plating buses 36 and 38 to bond posts 27 and solder pads 16, 19 and 51. Accordingly, *trace 32 in Sharma is not a voltage reference signal trace*. Further, Brooks reduces the self inductance through an increase in effective width and a decrease in the distance between the voltage reference plane and the traces. However, self inductance is generated by AC signals. Therefore, the problem going to be solved in Brooks is different from that in the present invention, i.e., a constant voltage input is provided to the voltage reference signal trace, therefore *the widen voltage reference signal trace is used to reduce parasitic resistance but not reduce self inductance*. Further, Honsinger does not even disclose a voltage reference signal trace in a non-signaling layer.

Accordingly, claim 27 is patentable over the citations, and, claims 28-33 are patentable over the citations as a matter of law since their depending claim 27 is patentable over the citations.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 16 and 27 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 17-22 and 28-33 patently define over the prior art as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 16-22 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : Dec. 21, 2004

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